



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,802	07/10/2003	Barinder Singh Rai	VP070	2294
20178	7590	10/07/2005	EXAMINER	
EPSON RESEARCH AND DEVELOPMENT INC INTELLECTUAL PROPERTY DEPT 150 RIVER OAKS PARKWAY, SUITE 225 SAN JOSE, CA 95134			FLOURNOY, HORACE L	
			ART UNIT	PAPER NUMBER
			2189	

DATE MAILED: 10/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/616,802	RAI ET AL.	
	Examiner	Art Unit	
	Horace L. Flournoy	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 10 July 2003.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-26 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 10 July 2003 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claims 1-26 are presented for examination.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1 recites "...configuration of a signal..." The specification does not enable one of ordinary skill in the art to know how to "attach importance" to something. In other words, what is the "configuration of a signal" doing? How is the configuration happening?

The examiner reminds the applicant that this "configuration of a signal" must be explained in the specification as originally filed, in accordance with 35 USC § 112, 1st paragraph.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3 and 4 recite the limitation "stored in the buffer" in line 2 of claims 3 and 4. There is insufficient antecedent basis for this limitation in the claim. Claim 1 recites, "...stored in the temporary data storage area..." in lines 8-9.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-16, 18-21, 23-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Blodgett (U.S. Patent no. 6,401,186 hereafter referred to as Blodgett).

With respect to independent claim 1,

"A method for optimizing memory bandwidth, comprising: requesting data associated with a first address; obtaining the data associated with the first address and data associated with a consecutive address from a memory region in a manner transparent to a microprocessor;"

Art Unit: 2189

Blodgett discloses in column 6, lines 62-67, "The column address generated in the absence of a request by the microprocessor can be determined in any number of ways." (Note: Blodgett further anticipates this limitation in column 7).

"...storing the data associated with the first address and data associated with the consecutive address in a temporary data storage area;" is disclosed in column 6, lines 33-38, and FIG. 2.

Blodgett discloses in column 6, lines 33-38, "A first column address (COLm) identified by the microprocessor 80 is provided to the memory 84. The first address is used as the starting address for the burst read operation. The internal address is advanced in either a sequential or interleaved manner as described above with reference to FIG. 2.

Blodgett teaches storing the data associated with the first address (first address used as the starting address) in a buffer (memory 84) and storing data associated with a consecutive address relative to the first address in the buffer (The internal address is advanced in a sequential manner).

"...requesting data associated with a second address; and" is disclosed in column 6, lines 21-29.

Blodgett discloses disclosed in column 6, lines 21-29, "...the microprocessor can be programmed such that the next address generated by the memory controller is known. This embodiment allows the microprocessor to use the new data without

requesting a read operation. The burst memory 84 can include an address generation circuit which determines the next address to be requested by the microprocessor. The memory controller, therefore, does not determine the next address.

"...determining whether the data associated with the second address is stored in the temporary data storage area through a configuration of a signal requesting the data associated with the second address." disclosed in column 3, lines 46-47, 66-67, column 4, lines 1-3, and FIG.3 (Note: see all signals).

Blodgett discloses in column 3, lines 66-67, column 4, lines 1-3 "For a burst write cycle, data 10 is latched in input data latches 34. Data targeted at the first address specified by the row and column addresses is latched with the CAS* signal. Blodgett also discloses in column 3, lines 46-47, "The column address may be advanced with each CAS* transition, or each pulse."

Blodgett teaches a signal (CAS*) that is issued for distributing the data associated with the address (first address) and the data associated with the consecutive address (The column address may be advanced with each CAS* transition, or each pulse).

With respect to claim 2,

"The method of claim 1, wherein the method operation of obtaining the data associated with the first address and data associated with a consecutive address from a memory region in a manner transparent to a microprocessor includes, completing the obtaining the data associated with the first address and data associated with a consecutive address in one clock cycle associated with the microprocessor." is disclosed in column 3, lines 15-18 and FIGs. 1, 3, 4, 6, and 7.

Blodgett discloses in column 3, lines 15-18, "In a burst read cycle, data within the memory array located at the row and column address selected by the row and column address decoders is read out of the memory array and sent along data path 32 to output latches 34."

Blodgett teaches completing the obtaining the data (read out of the memory array) associated with the first address and data associated with a consecutive address (memory array located at the row and column address selected) in one clock cycle associated with the microprocessor (See FIGs. 1, 3, 4, 6, and 7).

With respect to claim 3,

"The method of claim 1, wherein the method operation of determining whether the data associated with the second address is stored in the buffer through a configuration of a signal requesting the data associated with the second address includes, comparing the most significant bits of the signal to corresponding most significant bits of a previous signal; and if the most significant bits of the signal

are equal to the corresponding most significant bits of the previous signal, then the method includes, accessing the data in the temporary data storage area." is disclosed in column 6, lines 1-28 and column 4, lines 1-17.

The examiner interprets claim 3 to as a "hit" in temporary data storage or cache and therefore does not require a fetch for needed data in the memory region.

Blodgett discloses in column 6, lines 13-21, "The memory controller can include an address comparator which compares an address requested by the microprocessor and a new address generated by the memory controller. If the addresses are the same, the memory controller continues with the new burst read operation. If the address requested by the microprocessor is different from that produced by the memory controller, a new read operation is initiated at the address provided by the microprocessor."

Blodgett teaches that via the use of a comparator (to determine whether the data associated with the second address is stored in the buffer through a configuration of a signal requesting the data associated with the second address includes, comparing the most significant bits of the signal to corresponding most significant bits of a previous signal) if a "hit" occurs (if the most significant bits of the signal are equal to the corresponding most significant bits of the previous signal) then access the data in the temporary data storage area (If the addresses are the same, the memory controller continues with the new burst read operation).

With respect to claim 4,

"The method of claim 1, wherein the method operation of determining whether the data associated with the second address is stored in the buffer through a configuration of a signal requesting the data associated with the second address includes, comparing the most significant bits of the signal to corresponding most significant bits of a previous signal; and if the most significant bits of the signal are not equal to the corresponding most significant bits of the previous signal, then the method includes, fetching the data associated with the second address from the memory region; and fetching consecutive data associated with the second address from the memory region." is disclosed in column 6, lines 1-28 and column 4, lines 1-17.

The examiner interprets claim 3 to as a "miss" in temporary data storage or cache and therefore requires a fetch for the needed data in the memory region.

Blodgett discloses in column 6, lines 13-21, "The memory controller can include an address comparator which compares an address requested by the microprocessor and a new address generated by the memory controller. If the addresses are the same, the memory controller continues with the new burst read operation. If the address requested by the microprocessor is different from that produced by the memory controller, a new read operation is initiated at the address provided by the microprocessor."

Blodgett teaches that via the use of a comparator (to determine whether the data associated with the second address is stored in the buffer through a configuration of a

signal requesting the data associated with the second address includes, comparing the most significant bits of the signal to corresponding most significant bits of a previous signal) if a “miss” occurs (if the most significant bits of the signal are not equal to the corresponding most significant bits of the previous signal) then fetch the consecutive data associated with the second address from the memory region (. If the address requested by the microprocessor is different from that produced by the memory controller, a new read operation is initiated at the address provided by the microprocessor).

With respect to claim 5,

“The method of claim 4, further comprising: determining an amount of consecutive data to fetch according to a value associated with the least significant bits of the signal.” is disclosed in column 6, lines 62-67 – column 7, lines 1-8.

Blodgett discloses in column 6, lines 62-67 – column 7, lines 1-8, “The column address generated in the absence of a request by the microprocessor can be determined in any number of ways. The new address can be produced by repeating the prior sequence with an advanced most significant bit, as shown in Tables 1 where X represents address most significant bits (MSB's) followed by bits A1 and A0. In Table 1 an interleaved address sequence is shown for a burst length of 4. The next burst sequence start address is derived by incrementing the MSB's (X) and by repeating the

initial LSB's (A1, A0). In Table 2 the next burst sequence start address is derived by incrementing the MSB's and resetting the LSB's to 0, 0. Either of these methods may be utilized for other burst length options, and for other addressing sequences."

Blodgett teaches determining an amount of consecutive data (burst length) to fetch according to a value associated with the least significant bits (LSB) of the signal.

With respect to independent claim 6,

"A method for efficiently executing memory reads based on a read command issued from a central processing unit (CPU), comprising: requesting data associated with a first address in memory in response to receiving the read command;" is disclosed in column 1, lines 63-67 and column 2, lines 1-6.

Blodgett discloses in column 1, lines 63-67 and column 2, lines 1-2, "...a system comprising a synchronous memory device having addressable memory cells, a microprocessor coupled to the synchronous memory device for data communication with the addressable memory cells, the microprocessor further initiating a data read operation at a first memory cell address. A memory controller is connected to the microprocessor and the synchronous memory device."

"...storing the data associated with the first address in a buffer;

storing data associated with a consecutive address relative to the first address in the buffer," is disclosed in column 6, lines 33-38, and FIG. 2.

Blodgett discloses in column 6, lines 33-38, "A first column address (COLm) identified by the microprocessor 80 is provided to the memory 84. The first address is used as the starting address for the burst read operation. The internal address is advanced in either a sequential or interleaved manner as described above with reference to FIG. 2.

Blodgett teaches storing the data associated with the first address (first address used as the starting address) in a buffer (memory 84) and storing data associated with a consecutive address relative to the first address in the buffer (The internal address is advanced in a sequential manner).

"...the storing occurring prior to the CPU being capable of issuing a next command following the read command;" is disclosed in column 1, lines 44-46 and lines 62-67.

Blodgett discloses in column 1, lines 44-46 and lines 62-67, "a processor receiving data from a memory may delay a new memory read operation until a prior read is complete...In particular, the present invention describes a system comprising a synchronous memory device having addressable memory cells, a microprocessor coupled to the synchronous memory device for data communication with the addressable memory cells, the microprocessor further initiating a data read operation at a first memory cell address."

Blodgett teaches completing the storing (data in memory) prior to the microprocessor being capable of issuing any command following the read operation (delay a new memory read operation until a prior read is complete).

"...determining if a next read command corresponds to the data associated with the consecutive address; and if the next read command corresponds to the data associated with the consecutive address, the method includes, obtaining the data from the buffer." is disclosed in column 6, lines 62-67, column 7, lines 1-30 and TABLES 1 and 2.

Blodgett discloses in column 6, lines 62-67, "The column address generated in the absence of a request by the microprocessor can be determined in any number of ways." (Note: this limitation is further anticipated by Blodgett in column 7).

With respect to claim 7,

"The method of claim 6, further comprising: if the next read command does not correspond to the data associated with the consecutive address, the method includes, storing data associated with the next read command in the buffer; and storing data having a consecutive address to the data associated with the next read command in the buffer." is disclosed in column 6, lines 33-38, and FIG. 2.

Blodgett discloses in column 6, lines 33-38, "A first column address (COLm) identified by the microprocessor 80 is provided to the memory 84. The first address is

used as the starting address for the burst read operation. The internal address is advanced in either a sequential or interleaved manner as described above with reference to FIG. 2.

Blodgett teaches storing the data associated with the next read command (first address used as the starting address) in a buffer (memory 84) and storing data associated with a consecutive address relative to the first address in the buffer (The internal address is advanced in a sequential manner).

With respect to claims 9 and 10,

"The method of claim 6, wherein the method operation of storing data associated with a consecutive address relative to the first address in the buffer includes, issuing a read store select signal; and directing the data to a storage location of the buffer according to the read store select signal."

and

"The method of claim 6, wherein the method operation of obtaining the data from the buffer includes, determining a location of the data in the buffer through a data select signal." are disclosed in column 3, lines 46-47, 66-67, column 4, lines 1-3, and FIG.3 (Note: see all signals).

Blodgett discloses in column 3, lines 66-67, column 4, lines 1-3 "For a burst write cycle, data 10 is latched in input data latches 34. Data targeted at the first address specified by the row and column addresses is latched with the CAS* signal. Blodgett

Art Unit: 2189

also discloses in column 3, lines 46-47, "The column address may be advanced with each CAS* transition, or each pulse."

Blodgett teaches a signal (CAS*) that is issued for distributing the data associated with the address (first address) and the data associated with the consecutive address (The column address may be advanced with each CAS* transition, or each pulse).

With respect to independent claim 11,

"A memory controller, comprising: logic for requesting a read operation from memory; logic for generating an address for the read operation;" is disclosed in the abstract.

The examiner interprets the limitation "logic" as a device or a means for.

Blodgett discloses in the abstract, "A system is described which uses a burst access memory and a memory controller to anticipate the memory address to be used in future data read operations as requested by a microprocessor. Either the memory controller or the memory device initiates a burst read operation starting at a memory address generated thereby."

Blodgett teaches memory controller, comprising that comprises logic for requesting (initiates) a read operation from memory and generates an address for the read operation (burst read operation starting at a memory address generated thereby).

"...logic for storing both, data associated with the address and data associated with a consecutive address in temporary storage;" is disclosed in column 6, lines 33-38, and FIG. 2.

Blodgett discloses in column 6, lines 33-38, "A first column address (COLm) identified by the microprocessor 80 is provided to the memory 84. The first address is used as the starting address for the burst read operation. The internal address is advanced in either a sequential or interleaved manner as described above with reference to FIG. 2.

Blodgett teaches storing the data associated with the first address (first address used as the starting address) in a buffer (memory 84) and storing data associated with a consecutive address relative to the first address in the buffer (The internal address is advanced in a sequential manner).

"...and logic for determining if a request for data associated with a next read operation is for the data associated with the consecutive address in the temporary storage." is disclosed in column 1, lines 40-49.

Blodgett discloses in column 6 lines 1-9, "The present invention includes memory controller 82 which initiates a read operation at a memory address determined to be the most likely next address to be requested by the microprocessor 80. The memory controller, therefore, anticipates the next address to be requested by the microprocessor. If the microprocessor requests data from the memory which

corresponds to the new address determined by the memory controller, access time is saved."

Blodgett teaches logic for determining if a request for data associated with a next read operation (read operation at a memory address) is for the data associated with the consecutive address (next address) in the temporary storage (memory).

With respect to claims 12, 8, 18, and 24,

"The memory controller of claim 11, wherein the logic for determining if a request for data associated with a next read operation is for the data associated with the consecutive address in the temporary storage includes, a comparator configured to compare a signal corresponding to the request for data associated with a next read operation with a signal corresponding to the address for the read operation." is disclosed in column 6, lines 13-16 and column 8, lines 51-54.

Blodgett discloses in column 6, lines 13-16, "The memory controller can include an address comparator which compares an address requested by the microprocessor and a new address generated by the memory controller."

Blodgett teaches a comparator configured to compare a signal corresponding to the request for data associated with a next read operation (new address generated by the memory controller) with a signal corresponding to the address for the read operation

(address requested by the microprocessor). Blodgett further teaches that the memory controller is a buffer for the new address generated by itself.

With respect to claim 13,

"The memory controller of claim 11, wherein the logic for storing both, data associated with the address and data associated with a consecutive address in temporary storage is configured to issue a signal for distributing the data associated with the address and the data associated with the consecutive address in the temporary storage." is disclosed in column 3, lines 46-47, 66-67, column 4, lines 1-3, and FIG.3.

Blodgett discloses in column 3, lines 66-67, column 4, lines 1-3 "For a burst write cycle, data 10 is latched in input data latches 34. Data targeted at the first address specified by the row and column addresses is latched with the CAS* signal. Blodgett also discloses in column 3, lines 46-47, "The column address may be advanced with each CAS* transition, or each pulse."

Blodgett teaches a signal (CAS*) that is issued for distributing the data associated with the address (first address) and the data associated with the consecutive address (The column address may be advanced with each CAS* transition, or each pulse).

Art Unit: 2189

With respect to claim 14,

"The memory controller of claim 11, wherein the logic for requesting a read operation from memory originates from a microprocessor." is disclosed in column 1, lines 64-67 and column 2, lines 1-6.

Blodgett discloses in column 1, lines 64-67 and column 2, lines 1-6, "...a microprocessor coupled to the synchronous memory device for data communication with the addressable memory cells, the microprocessor further initiating a data read operation at a first memory cell address. A memory controller is connected to the microprocessor and the synchronous memory device. The memory controller produces a second memory cell address and initiates a read operation in anticipation of a second data read operation at a new memory cell address provided from the microprocessor."

With respect to claim 15,

"The memory controller of claim 14, wherein the logic for storing both, data associated with the address and data associated with a consecutive address in temporary storage includes, completing the storing prior to the microprocessor being capable of issuing any command following the read operation." is disclosed in column 1, lines 44-46 and lines 62-67.

Blodgett discloses in column 1, lines 44-46 and lines 62-67, "a processor receiving data from a memory may delay a new memory read operation until a prior read

is complete...In particular, the present invention describes a system comprising a synchronous memory device having addressable memory cells, a microprocessor coupled to the synchronous memory device for data communication with the addressable memory cells, the microprocessor further initiating a data read operation at a first memory cell address."

Blodgett teaches completing the storing (data in memory) prior to the microprocessor being capable of issuing any command following the read operation (delay a new memory read operation until a prior read is complete).

With respect to independent claim 16,

"An integrated circuit, comprising: circuitry for issuing a command memory circuitry in communication with the circuitry for issuing the command, the memory circuitry including," is disclosed in column 1, lines 63-67 and column 2, lines 1-6.

Blodgett discloses in column 1, lines 63-67 and column 2, lines 1-2, "...a system comprising a synchronous memory device having addressable memory cells, a microprocessor coupled to the synchronous memory device for data communication with the addressable memory cells, the microprocessor further initiating a data read operation at a first memory cell address. A memory controller is connected to the microprocessor and the synchronous memory device."

Blodgett teaches an integrated circuit, that comprises circuitry for issuing a command (microprocessor) memory circuitry (synchronous memory device) in communication with the circuitry for issuing the command (a microprocessor coupled to the synchronous memory device for data communication with the addressable memory cells).

"...a random access memory (RAM) core circuitry;" is disclosed in column 7, lines 31-32, and FIGs. 5 and 8.

Blodgett discloses in column 7, lines 31-32, "FIG. 8 illustrates one operation of the system of an SDRAM which can be used in the system of FIG. 5."

"...a memory controller configured to issue a first request for data associated with an address of the RAM, the memory controller further configured to issue a second request for data associated with a consecutive address to the address;" is disclosed in column 2, lines 18-30.

Blodgett discloses in column 2, lines 18-30, "The method comprises the steps of providing a read request from a microprocessor, the read request including a memory cell start address for the synchronous memory device. The method further including the steps of initiating a read operation using a memory controller in response to the read request, and outputting data from the synchronous memory device in response to the memory controller. A new memory address is generated in anticipation of a second read request from the microprocessor, the second read request including a second

memory cell start address. Finally, a second read operation is initiated and data is output from the synchronous memory device starting at the new memory address."

"...and a buffer in communication with the memory controller, the buffer configured to store the data associated with the address and the consecutive address in response to the respective requests for data, the data associated with the address and the consecutive address being stored prior to a next command being issued," is disclosed as stated *supra*.

(Note: the examiner interprets the usage of the memory controller or the burst memory as buffers in communication with the memory controller.)

"...wherein the memory controller includes circuitry configured to determine whether the second request is for the data associated with the consecutive address." is disclosed in column 6, lines 13-16.

Blodgett discloses in column 6, lines 13-16, "The memory controller can include an address comparator which compares an address requested by the microprocessor and a new address generated by the memory controller."

With respect to claim 19,

"The integrated circuit of claim 16, wherein the core circuitry is configured as synchronous dynamic random access memory (SDRAM) circuitry." is disclosed in column 7, lines 31-32, and FIGs. 5 and 8.

Blodgett discloses in column 7, lines 31-32, "FIG. 8 illustrates one operation of the system of an SDRAM which can be used in the system of FIG. 5."

With respect to claims 20 and 23,

"The integrated circuit of claim 16, wherein the memory controller includes selection and storage logic configured to enable one of distribution of the data associated with the address and the consecutive address into the buffer, and access to the data associated with the address and the consecutive address from the buffer." is disclosed in column 6, lines 53-61.

The examiner interprets claim to mean that distribution for either the data address or the consecutive data address is enabled based on selection logic. The storage logic is implemented for access of the address and the consecutive address from the buffer. (Note: this limitation is interpreted as analogous to claim 11, and is therefore stated supra)

Blodgett discloses in column 6, lines 53-61, "...the present invention can include an address generator internal to the memory control circuitry 38 which produces a new column address if a valid new address is not provided on the external address lines. To assist the memory controller, the output enable (OE*) input can be used to indicate the

presence of a valid address on the address lines. Further, additional counter circuitry can be added to the memory to enable the memory to output a full length column sequence."

Blodgett teaches the distribution for either the data address or the consecutive data address (both on address lines) is enabled based on selection logic (the output enable (OE*) input can be used to indicate the presence of a valid address on the address lines).

With respect to independent claim 21,

"A device, comprising: a graphics processing unit (GPU)" is disclosed in column 1, lines 63-67 and column 2, lines 1-6.

The examiner interprets a graphics processing unit (GPU) as a CPU or microprocessor, which is admitted as an equivalent by applicant in the specification (lines 20-21 of page 8). As per MPEP 2144 and 2173.05, a graphic processing unit as disclosed by the applicant is a functional limitation that does not distinguish from prior art in terms of structure rather than function alone.

Blodgett discloses in column 1, lines 63-67 and column 2, lines 1-2, "...a system comprising a synchronous memory device having addressable memory cells, a microprocessor coupled to the synchronous memory device for data communication with the addressable memory cells, the microprocessor further initiating a data read

operation at a first memory cell address. A memory controller is connected to the microprocessor and the synchronous memory device."

"...a memory region in communication with the GPU over a bus," is disclosed as stated supra in claim 16.

"...the memory region configured to receive a read command from the GPU, the memory region including, a read buffer for temporarily storing data; and a memory controller in communication with the read buffer, the memory controller configured to issue requests for one of fetching data in memory having an address associated with the read command and fetching data in memory associated with a consecutive address to the address, in response to receiving a read command from the GPU, wherein the requests cause the data associated with the consecutive address to be stored in the read buffer prior to the GPU issuing a next command after the read command." is disclosed as stated supra.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere CO.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 17 and 22 are rejected under 35 U.S.C. 103(a) as being obvious over Blodgett (U.S. Patent no. 6,401,186) in view of Oberlaender et al. (US Patent No. 6,507,899 hereafter referred to as Oberlaender).

With respect to claims 17 and 22, Blodgett teaches "The integrated circuit of claim 16..." as stated supra.

Blodgett, however, does not disclose expressly "...wherein the memory circuitry further comprises: a first multiplexer configured to distribute the data associated with the address and the data associated with the consecutive address into the buffer; and a second multiplexer configured to select the data associated with the consecutive address when the second request is for the data associated with the second address."

Oberlaender discloses in column 1, lines 55-66, "The interface circuit comprises an address buffer having an input and an output, whereby the input receives an address

Art Unit: 2189

signal from the data handling unit, a first multiplexer which couples the memory unit with either the output of the address buffer or with the address signal, a data buffer having an input and an output, the input receiving a data signal from the data handling unit and the output being coupled with the memory data input, a second multiplexer for selecting either the memory data signal output or the data buffer output, and a comparator for comparing the address signal with the signal from the address buffer output, generating a control signal which controls the second multiplexer."

Oberlaender further discloses in column 8, lines 15-28, "The next cycle is assumed to be a read cycle R3. During this cycle the now incoming data and control signals from the previous write cycle are buffered in registers 512 and 530. The previously stored address is copied from register 504 into register 503. The new incoming address is fed to the SRAM through multiplexer 500 which is switched to input 1 and stored in register 504. Comparator 505 compares the content of registers 504 and 503. In this case they are different. Therefore, multiplexer 520 is switched to input 0 and feeds the data read from the SRAM to the output D.sub.out'. Multiplexer 531 is switched to input 1 to couple the control signal WE' with the respective control input of the SRAM.

Blodgett and Oberlaender are analogous art because they are from the same field of endeavor, that being devices for processing data.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine a first multiplexer configured to distribute the data associated with the address and the data associated with the consecutive address into the buffer;

and a second multiplexer configured to select the data associated with the consecutive address when the second request is for the data associated with the second address, with the integrated circuit of claim 16 (or device of claim 21).

The motivation for doing so would have been obvious based on the teaching of Oberlaender in column 1, lines 5-42, "One of the main factors, which determine the speed of a microprocessor, is defined by the interface between the central processing unit and the memory...As in a reading instruction data will be provided by the memory, only the memory access delay occurs and reading instructions can be executed in one cycle..."

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention having the teachings of Blodgett and Oberlaender before him/her to combine Oberlaender and Blodgett for the benefit of combine a first multiplexer configured to distribute the data associated with the address and the data associated with the consecutive address into the buffer; and a second multiplexer configured to select the data associated with the consecutive address when the second request is for the data associated with the second address, with the integrated circuit of claim 16 (or device of claim 21) to obtain the invention as specified in Claims 17 and 22.

Claims 25 and 26 are rejected under 35 U.S.C. 103(a) as being obvious over Blodgett (U.S. Patent no. 6,401,186) in view of Le Pennec et al. (US Patent No. 6,920,488 hereafter referred to as Le Pennec).

With respect to claims 25 and 26, Blodgett teaches "The device of claim 21..." as stated supra.

Blodgett, however, does not disclose expressly "...wherein the device is a portable handheld electronic device." or "...further comprising: a display screen configured to display image data."

Le Pennec discloses in column 4, lines 21-24, "The behavior of the PDA can be simulated on the portal server using a normal web browser. A web page further can demonstrate the operability of the PDA screen and buttons." Le Pennec teaches a portable handheld electronic device (PDA or personal digital assistant) and also a display screen configured to display image data (PDA screen).

Blodgett and Le Pennec are analogous art because they are from the same field of endeavor, that being devices for processing data.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine a portable handheld electronic device (with a display screen configured to display image data) with the device of claim 21.

The motivation for doing so would have been obvious based on the teaching of Le Pennec in column 4, lines 11-15, "fields may be selected for viewing alone on the screen either by selecting the field by the pen of the PDA, or otherwise identifying the input field depending upon the capabilities of the PDA." Le Pennec also discloses in column 1, lines 12-14, "A Personal Digital Assistant which is a simple and small device fitting in the pocket, combines the portability..."

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention having the teachings of Blodgett and Le Pennec before him/her to combine Le Pennec and Blodgett for the benefit of having a portable handheld electronic device (with a display screen configured to display image data) with the device of claim 21 to obtain the invention as specified in Claims 25 and 26.

Conclusion

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Horace L. Flournoy whose telephone number is (571) 272-2705. The examiner can normally be reached on Monday-Friday 7:00 AM to 4:30 PM (ET).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Don Sparks can be reached on (571) 272-4201. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 746-7239

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Art Unit: 2189

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

Horace L. Flournoy



Patent Examiner

Art unit: 2189

Primary Patent Examiner

Technology Center 2100



CHRISTIAN CHACE
PRIMARY EXAMINER